CLAIMS

1. A comparator for an analog-to-digital converter comprising:
- an input for receiving an input signal;
- a bipolar latch stage coupled to the input for performing a latch decision based on said input signal and for outputting an output signal depending on said decision;
- a reset switch coupled to said bipolar latch stage for resetting said latch stage subsequent to said latch decision;
- amplification means coupled to the latch stage for amplifying said output signal so that said amplified output signal is suitable to be input to CMOS circuitry,
wherein said amplification means includes:
- a first tapping or level shift transistor coupled to said bipolar latch stage for, depending on the latch decision, tapping a collector current from said latch stage, while leaving the latch decision thereof unaffected, so that a current gain of said bipolar latch stage can be used to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said output signal.

2. The comparator as claimed in claim 1 wherein said input includes a pair of differential inputs, and wherein said input signal is a differential input signal.

3. The comparator as claimed in claim 2 wherein said output signal is a differential output signal, and wherein said amplification means includes a second tapping or level shift transistor coupled to said bipolar latch stage for, depending on the latch decision, tapping a collector current from said latch stage, while leaving the latch decision thereof unaffected, such that a current gain of said bipolar latch stage can be used to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said differential output signal.

4. The comparator as claimed in claim 3 wherein said pair of tapping or level shift transistors are bipolar transistors.

5. The comparator as claimed in claim 3 wherein said bipolar latch stage includes a pair of bipolar transistors, the base of each of which is coupled to the emitter of a respective one of said tapping or level shift transistors.

6. The comparator as claimed in claim 5 wherein said comparator is adapted to turn off one of said bipolar latch transistors subsequent to said latch decision to thereby switch a bias current fed into said one bipolar latch transistor to the base of the other one of said bipolar latch transistors, whereby a collector current of said other one of said bipolar latch transistors will be considerably increased.

7. The comparator as claimed in claim 3 wherein said comparator is adapted to directly lead said tapped collector current from said latch stage via one of said tapping or level shift transistors to one of said differential outputs.

8. The comparator as claimed in claim 3 wherein each of said differential outputs is coupled to an inverter.

9. The comparator as claimed in claim 3 wherein said comparator is implemented in BiCMOS technology.

10. The comparator as claimed in claim 3 wherein the bipolar latch stage comprises a first and a second bipolar transistor arranged in a cross-coupled state, so that
- the collector of the first transistor is connected to the base of the second transistor, which connection defines a first node; and
- the collector of the second transistor is connected to the base of the first transistor, which connection defines a second node; and wherein
- the emitters of the first and second transistors are connected to a common electrical potential.

11. The comparator as claimed in claim 10 wherein said pair of differential inputs are connected, via said input stage, to said first and second nodes, respectively.

12. The comparator as claimed in claim 10 wherein
- a first one of said pair of tapping or level shift transistors is connected so that the emitter thereof is connected to said first node, and the collector thereof is connected, via a third node, to a first one of said pair of differential outputs; and
- a second one of said pair of tapping or level shift transistors is connected so that the emitter thereof is connected to said second node, and the collector thereof is connected, via a fourth node, to a second one of said pair of differential outputs; and wherein
- the bases of said pair of tapping or level shift transistors are connected.

13. The comparator as claimed in claim 12 further comprising a bias circuitry for biasing of the base voltage of said pair of tapping or level shift transistors.

14. The comparator as claimed in claim 3 wherein the bipolar latch stage comprises a first and a second bipolar transistor arranged so that
- the collector of the first transistor is connected to the base of a first one of said pair of tapping or level shift transistors, which connection defines a first node;
- the collector of the second transistor of the bipolar latch stage is connected to the base of a second one of said pair of tapping or level shift transistors, which connection defines a second node;
- the base of the first transistor is connected to the emitter of the second one of said pair of tapping or level shift transistors;
- the base of the second transistor of the bipolar latch stage is connected to the emitter of the first one of said pair of tapping or level shift transistors; and
- the emitters of the first and second transistors are connected to a common electrical potential.

15. The comparator as claimed in claim 14 wherein said pair of differential inputs are, via said input stage, connected to said first and second nodes, respectively.

16. The comparator as claimed in claim 14 wherein
- the collector of said first one of said pair of tapping or level shift transistors is connected, via a third node, to a first one of said pair of differential outputs; and
- the collector of said second one of said pair of tapping or level shift transistors is connected, via a fourth node, to a second one of said pair of differential outputs.

17. The comparator as claimed in claim 1 wherein said bipolar latch stage comprises four bipolar transistors in a Darlington-coupled state.

18. The comparator as claimed in claim 3 wherein
- said bipolar latch stage comprises four bipolar transistors, wherein
- the collector of a first one of said four bipolar transistors is connected to the base of a second one of said four bipolar transistors, which connection is further connected to the emitter of a first one of said pair of tapping or level shift transistors;
- the collector of a third one of said four bipolar transistors is connected to the base of a fourth one of said four bipolar transistors, which connection is further connected to the emitter of a second one of said pair of tapping or level shift transistors; and
- the collectors of said second and forth ones of said four bipolar transistors are connected to a voltage supply via an RC circuitry.

19. The comparator as claimed in claim 1 further comprising an input stage coupled to the input for receiving said input signal as a signal suitable for switched capacitor circuits.

20. The comparator as claimed in claim 19 wherein said input stage is adapted to supply said latch stage with bias current.

21. The comparator as claimed in claim 1 further comprising a clock for controlling said reset switch.

22. An analog-to-digital converter comprising a plurality of comparators wherein each comparator comprises:

- an input for receiving an input signal;
- a bipolar latch stage coupled to the input for performing a latch decision based on said input signal and for outputting an output signal depending on said decision;
- a reset switch coupled to said bipolar latch stage for resetting said latch stage subsequent to said latch decision;
- amplification means coupled to the latch stage for amplifying said output signal so that said amplified output signal is suitable to be input to CMOS circuitry,

wherein said amplification means includes:

- a first tapping or level shift transistor coupled to said bipolar latch stage for, depending on the latch decision, tapping a collector current from said latch stage, while leaving the latch decision thereof unaffected, so that a current gain of said bipolar latch stage can be used to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said output signal.

23. A method of operating a comparator for an analog-to-digital converter comprising the steps of:
- feeding an input signal to an input;
- performing a latch decision based on said input signal and outputting an output signal depending on said decision by means of a bipolar latch stage coupled to the input;
- resetting said latch stage subsequent to said latch decision by means of a reset switch coupled to said bipolar latch stage;
- amplifying said output signal, so that said amplified output signal is suitable to be input to CMOS circuitry; and
- outputting said output signal suitable to be input to CMOS circuitry,
said method being further comprising the steps of:
- depending on said latch decision tapping a collector current from said latch stage, while leaving the latch decision thereof unaffected, by means of a tapping or level shift transistor coupled to said bipolar latch stage; and
- using a current gain of said bipolar latch stage to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said output signal.

24. The method as claimed in claim 23 wherein said fed input signal is a differential input signal and said input includes a pair of differential inputs.

25. The method as claimed in claim 24 wherein said output signal is a differential output signal, and wherein, depending on said latch decision, a collector current is tapped from said latch stage by means of a second tapping or level shift transistor coupled to said bipolar latch stage, while leaving the latch decision thereof unaffected, so that a current gain of said bipolar latch stage can be used to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said differential output signal.

26. The method as claimed in claim 25 wherein

- said bipolar latch stage includes a pair of bipolar transistors; and wherein

- one of said bipolar latch transistors is turned off subsequent to said latch decision to thereby switch a bias current fed into said one bipolar latch transistor to the base of the other one of said bipolar latch transistors, whereby a collector current of said other one of said bipolar latch transistors will be considerably increased.

27. The method as claimed in claim 26 wherein said considerably increased collector current is directly lead from said other one of said bipolar latch transistors via one of said tapping or level shift transistors to one of said differential outputs.

28. A method of operating an analog-to-digital converter comprising the step of operating a plurality of comparators, wherein the operation of each comparator comprises the steps of:

- feeding an input signal to an input;
- performing a latch decision based on said input signal and outputting an output signal depending on said decision by means of a bipolar latch stage coupled to the input;
- resetting said latch stage subsequent to said latch decision by means of a reset switch coupled to said bipolar latch stage;
- amplifying said output signal, so that said amplified output signal is suitable to be input to CMOS circuitry; and
- outputting said output signal suitable to be input to CMOS circuitry,

said method being further comprising the steps of:

- depending on said latch decision tapping a collector current from said latch stage, while leaving the latch decision thereof unaffected, by means of a tapping or level shift transistor coupled to said bipolar latch stage; and
- using a current gain of said bipolar latch stage to amplify a latch bias current of said bipolar latch stage to thereby provide for the amplification of said output signal.